

# Claims

- [c1] 1. A fabrication method for a semiconductor device, comprising:  
forming a gate dielectric layer on a substrate;  
forming a plurality of gate structures on the substrate, wherein each gate structure comprises a gate conductive layer, a cap layer and a spacer;  
forming a mask layer on the substrate to cover some of the gate structures;  
removing the cap layer and the spacer of the gate structures that are not covered by the mask layer;  
removing the mask layer; and  
depositing a first dielectric layer on the substrate to cover the gate structures.
- [c2] 2. The method of claim 1, wherein the mask layer is formed to cover the gate structures where a self-aligned contact is subsequently formed or the gate structures on the active region.
- [c3] 3. The method of claim 2, wherein the mask layer is formed to cover a part of the gate structures.
- [c4] 4. The memory cell of claim 1, wherein the step of re-

moving of the cap layer and the spacer further comprises concurrently removing the cap layer of the gate structures at a predetermined site for a gate contact.

- [c5] 5. The method of claim 1, wherein after the step of removing the mask layer, the method further comprises a metal silicide fabrication process to form a metal silicide layer on an exposed sidewall of the gate conductive layer.
- [c6] 6. The method of claim 1, wherein a dielectric constant of the first dielectric layer is lower than a dielectric constant of the cap layer and the spacer.
- [c7] 7. The method of claim 1, wherein an etching selectivity ratio of the cap layer and the spacer to the gate dielectric layer and the gate conductive layer is greater than 10.
- [c8] 8. The method of claim 1, wherein after the step of forming the first dielectric layer, the method further comprises forming a self-aligned contact in the first dielectric layer and forming a conductive line on the first dielectric layer to electrically connect with the self-aligned contact.
- [c9] 9. The method of claim 1, wherein before forming the mask layer on the substrate, the method further comprises forming a second dielectric layer to fill between

the gate structures.

- [c10] 10. The method of claim 9, wherein after the step of removing the mask layer, the method further comprises forming a self-aligned contact in the first dielectric layer and the second dielectric layer, and forming a conductive line on the first dielectric layer to electrically connect with the self-aligned contact.
- [c11] 11. The method of claim 9, wherein the step of removing the cap layer of the gate structures not covered by the mask layer further comprises removing the spacer of the gate structures not covered by the mask layer to form a gap between a sidewall of the gate structures and the second dielectric layer.
- [c12] 12. The method of claim 11, wherein the step of forming the first dielectric layer to cover the gate structures further comprises forming voids in the first dielectric layer in the gap.
- [c13] 13. A fabrication method for a semiconductor device, comprising:  
forming a gate dielectric layer on a substrate;  
forming a plurality of gate structures on the substrate, wherein each gate structure comprises a gate conductive layer, a cap layer and a spacer;

filling a first dielectric layer in between the gate structures;  
forming a self-aligned contact in the first dielectric layer in between two of the gate structures;  
removing the cap layer of the gate structures; and  
forming a second dielectric layer on the first dielectric layer.

[c14] 14. The method of claim 13, wherein the step of removing the cap layer further comprises concurrently removing the cap layer of the gate structures at a predetermined site for forming a gate contact.

[c15] 15. The method of claim 13, wherein the step of removing the cap layer of the gate structures further comprises removing the spacer of the gate structures to form a gap at a sidewall of the gate structures.

[c16] 16. The method of claim 15, wherein the step of forming the second dielectric layer on the first dielectric layer further comprises forming voids in the second dielectric layer that is formed in the gap.

[c17] 17. The method of claim 13, wherein a dielectric constant of the second dielectric layer is lower than a dielectric constant of the cap layer and the spacer.

[c18] 18. The method of claim 13, wherein an etching selectiv-

ity between the cap layer and the spacer and the gate dielectric layer and the gate conductive layer is greater than 10.

[c19] 19. The method of claim 13, wherein after the step of forming the second dielectric layer, the method further comprises forming a conductive line on the second conductive layer to electrically connect with the self-aligned contact.

[c20] 20. A semiconductor device structure, the structure comprising:  
a gate dielectric layer, disposed on a substrate;  
a plurality of first gate structures, disposed on the gate dielectric layer, wherein the first gate structures comprise a gate conductive layer, a cap layer and a spacer;  
a plurality of second gate structures, disposed on the substrate, wherein the second gate structures comprise the gate conductive layer;  
a dielectric layer, disposed on the substrate, covering the first and the second gate structures;  
a self-aligned contact, disposed in the dielectric layer between the first gate structures; and  
a conductive line, disposed on the dielectric layer, wherein the conductive line electrically connects with the self-aligned contact.

- [c21] 21. The structure of claim 20, wherein the cap layer and the spacer of the first gate structures are disposed between the self-aligned contact and the gate conductive layer.
- [c22] 22. The structure of claim 20, wherein the dielectric layer at a sidewall of the gate conductive layer of the second gate structures comprises voids therein.
- [c23] 23. The structure of claim 22, wherein the dielectric layer at a sidewall of the gate conductive layer of the first gate structures that is not adjacent to the self-aligned contact comprises voids therein.
- [c24] 24. The structure of claim 20, wherein the second gate structures further comprise a spacer, disposed on a sidewall of the second gate structures, wherein the spacer is higher than the gate conductive layer.
- [c25] 25. The structure of claim 20, wherein a dielectric constant of the dielectric layer is lower than a dielectric constant of the cap layer and the spacer.
- [c26] 26. The structure of claim 20 further comprising a metal silicide layer formed on a sidewall of the gate conductive layer of the second gate structures.
- [c27] 27. The structure of claim 26, wherein a sidewall of the

gate conductive layer of the first gate structures that is not adjacent to the self-aligned contact further comprises the metal silicide layer.

[c28] 28. A semiconductor device structure, comprising:  
a gate dielectric layer, disposed on a substrate;  
a plurality of first gate structures, disposed on the gate dielectric layer, wherein the first gate structures comprise a gate conductive layer;  
a plurality of second gate structures, disposed on the substrate, wherein the second gate structures comprise the gate conductive layer;  
a dielectric layer disposed on the substrate, covering the first and the second gate structures;  
a self-aligned contact, disposed in the dielectric layer between the first gate structures, and the self-aligned contact and the first gate structures comprise the dielectric layer therebetween; and  
a conductive line, disposed on the dielectric layer, wherein the conductive line electrically connects with the self-aligned contact.

[c29] 29. The structure of claim 28, wherein the dielectric layer at a sidewall of the gate conductive layer of the first and the second gate structures comprises voids therein.

[c30] 30. The structure of claim 28 further comprising a

spacer, disposed on the sidewall of the conductive layer of the first gate structures and the second gate structures, wherein the spacer is higher than the conductive layer of the gate structure.

- [c31] 31. The structure of claim 30, wherein a dielectric constant of the dielectric layer is lower than a dielectric constant of the spacer.